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Design Deep Submicron Technology Architecture of High Speed Pseudo n-MOS Level Conversion Flip-Flop

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Abstract: Power has become primary constraint for both high performance and portable system designing, as a remedy using Dual-supply voltage design and Cluster Voltage Scaling scheme is an effective to reduce power consumption. In this thesis, simulated different Deep Submicron Technologies with multiple scaling methods to identify the effects on power dissipation and propagation delay of the CMOS circuit and achieved make trade of between Power Delay Product (PDP) with 180nm, 130nm, 90nm and 65nm technologies by implementing a design of Clock Sharing Pseudo n-MOS Level Conversion Flip-Flop (LCFF) which combines Pseudo n-MOS, Conditional Discharge and clocked switching concept with low power dissipation and delay overhead using pseudo n-MOS techniques. By using 65nm deep submicron technology, PDP enhanced by approximately 50% as observed from simulation results.

Index Terms—LCFF, Dual Supply, CVS, Pseudo n-MOS logic, Deep Submicron Technologies, Cosmos Scope, HSPICE (LEVEL 49 BSIM3 Version 3)

1 INTRODUCTION

Device scaling is an important part of VLSI design, which results in the faster integration of the circuit. As technology, moving towards Deep sub-micron region the circuit reliability is becoming a major issue. However, VLSI design must keep both power dissipation and circuit performance in balance with the scaling of devices. One of the most effective ways to reducing power dissipation is to reduce supply voltage. Since lowering supply voltage, it leads to increases the delay of circuit.

In order to reduce the supply voltage without compromising the system performance and circuit area, a Clustered Voltage Scaling (CVS) technique was develop in which critical and non-critical paths have clustered. It gives advantage by allowing modules to the critical path to use higher supply voltage levels V_{DDH} in speed sensitive paths so that speed will not effect, and allowing modules on non critical path to use low supply voltage, as a results whole system power dissipation could be reduced without performance degradation[2, 3]. Level converting flip-flop provides energy saving to the clock distribution network by using low swing clock signal but it makes delay overhead.

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In this system, level conversion is required in order to interface from (V_{DDL}) to (V_{DDH}) supply domains. However, the low supply cannot turn on the p-MOS devices at the Pull up network it makes delay overhead due at the level conversion. In order to reduce delay overhead of level conversion, the low supply voltage (V_{DDL}) followed with pipeline flip-flops, So that the level conversion has merged with flip-flop). Hence, it simultaneously performance latching and level conversion, it is called as Level Conversion Flip-Flop (LCFF) [1, 4].

One of the major issues in this thesis work is to design efficient LCFF which keep balanced in both power dissipation and circuit performance with the scaling of devices.

Total Power dissipated occurs in the circuit during transition and steady state periods is,

$$P_{total} = P_{active} + P_{leak} = P_{dynamic} + p_{sc} + p_{leak} \quad (1)$$

$$= \alpha f C_{eff} V_{dd}^2 + I_{sc} V_{dd} + I_{off} V_{dd} \quad (2)$$

Active power dissipated during transition period and it comprised with two parameters, dynamic power $P_{dynamic}$ (due charging and discharging the capacitance) and short circuit power P_{sc}(when direct path between VDD and GND).The leakage power has consumed during steady-state period or stand-by mode P_{leak} (when logic states remains constant and regarded as parasitic power) [1,4]. From the above equations, it is clear that by lowering supply voltage the power dissipation of the circuits will reduce due to the quadric relation between dynamic power and supply voltage because power has become primary constraints of both high performance and portable of system design.

2 TECHNOLOGY EVOLUTION

As the demand for high speed, low power consumption and packing density continuously growing in every year, so there is need a to scale down the devices to small dimensions and improve the reliability of IC component. Scaling the supply voltage for digital circuits has been the most effective way to lower the power dissipation because it reduces all power.

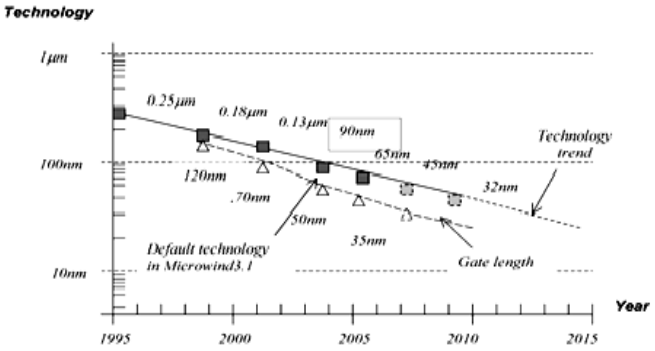


Fig 2.1 Technology scale down to NANO scale devices

From the above Fig 2.1, it is clear that as the physical gate length is slightly smaller than the technology node, the linear dimensions have approximately reduced by a factor of 0.7 and the area has reduced by a factor of 2.

- Scaling brings following benefits:
- Improved device characteristics
- Reduced the capacitance
- Improve interconnect technology

As the technology scale down in every two years due to increases the number of devices in circuit like supply, gate length and lambda get vary according to the technology used. Table 1.1 gives the overview parameters used for technology from 180nm technology introduced in 1999, scale down up to 14nm technology that have introduced in the year of 2014. However scaling dimensions and the supply voltage have to decrease to limit the field strength in the insulator, this decrease leads to tremendous increase in propagation delay.

3 LEVEL CONVERSION SCHEMES

Level Conversion Flip-Flop (LCFF) provides energy saving to the clock distribution network by using low swing clock signal but it makes delay overhead. Major issue of thesis Design is an efficient LCFF with fewer powers and delay overhead.

Different level shifting schemes has developed from time to time.

3.1 Differential Level Conversion Scheme

In this scheme the input is give through Differential Cascade Voltage Switch (DCVS) logic. There are two pull up networks one for each true and complement output, Each pull down network have a one p-type pull-up and those pull-up networks are cross-coupled.

There are two techniques implemented using differential method. Slave Latch Level Shifting Scheme (SLLS), this scheme causing large delay and power consumption especially true if it is voltage of clock at input signals are low swing and Clock Level Shifted Sense Amplifier (CSSA) uses a cross-coupled NAND gates at the set and reset the latch that results in output delay and that limits the performance of the flip-flop. The main drawback of this scheme is large power consumption and delay overhead due to crossover contention [1, 5].

3.2 Pre-charged Level Shifting Scheme

Pre-charged circuits offer both low area and higher speed but pre-charged gates introduce functional complexity because they operate in two distinct phases [7, 8].

There are two schemes implemented using Pre-charging method. Pulse Pre-charging (PPR) LCFF, this scheme will not contribute the necessary level conversion due to switching activity with pre-charging device it causes the redundant power and delay overhead. In order resolve this problem, clocked transistor switching activity the new technique as proposed self pre-charging flip-flop (SPFF) scheme, this scheme removes the need for a clock signal to drive p-MOS pre-charged transistors. Since the drawback of this scheme is, the last two inverters (I1, I2) incorporate power consumption and delay overhead.

3.3 NMOS Pass Transistor Scheme

Fig. 3.3.1 shows the structure of NMOS-pass transistor scheme. It reduces the number of active devices by eliminating redundant switching transistors, where transistor used as a switch to pass the logic level between nodes instead of switches directly connected to the supply voltage.

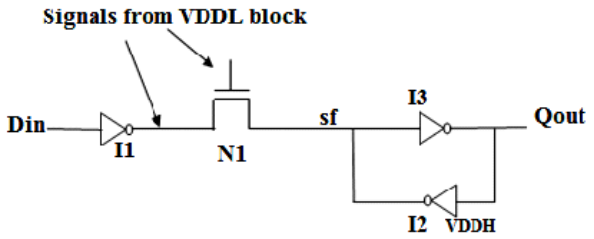


Fig 3.3.1 n-MOS Pass Transistor Scheme

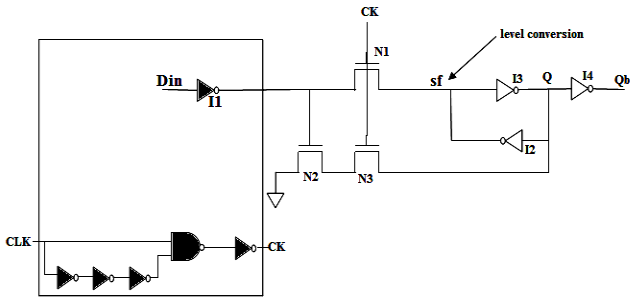


Fig 3.3.1.1 Pulse Half Latch (PHL) Level Shifting Scheme

3.3.1 Pulse Half Latch (PHL) LCFF

In order to resolve this problem the new technique Pulse Half Latch (PHL) LCFF is proposed, which uses the

n-MOS-pass transistor logic and the structure as shown in Fig 3.3.1.1 [1, 6].

PHL level shifting scheme is an efficient design among all techniques developed with differential, pre-charging and n-MOS Pass transistor schemes because PHL scheme consume less power (15.353u) consumption but delay (345.87p) increased due to threshold drop. Simulation results as shown in below Fig 3.3.1.2(a) and Fig 3.3.1.2(b).

3.3.1.1 Simulation Results of PHL-LCFF

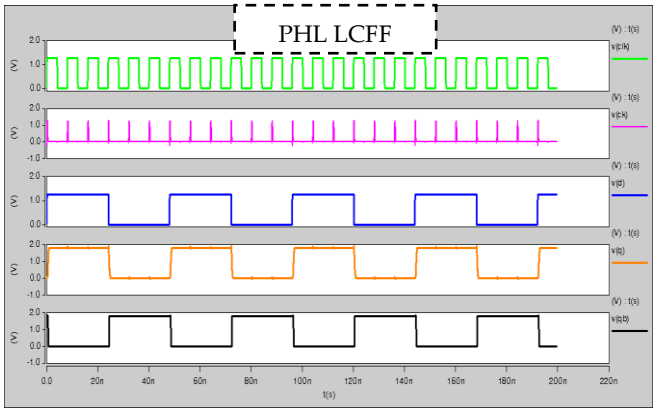


Fig 3.3.1.1(a) Results of Data to Output for PHL-LCFF

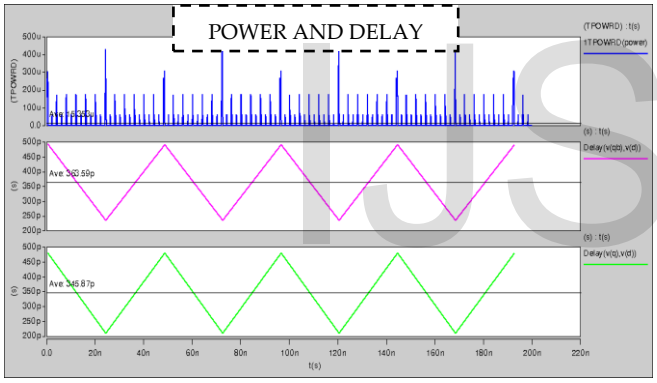


Fig 3.3.1.1 (b) Results of Power and Delay for PHL-LCFF

However, it has similar drawback threshold voltage drop due to the pass transistor N1 and two transistor connected in series N1 and N2 must be strong enough to pull down quickly but it takes two gates of delay hence it resulting in delay overhead .

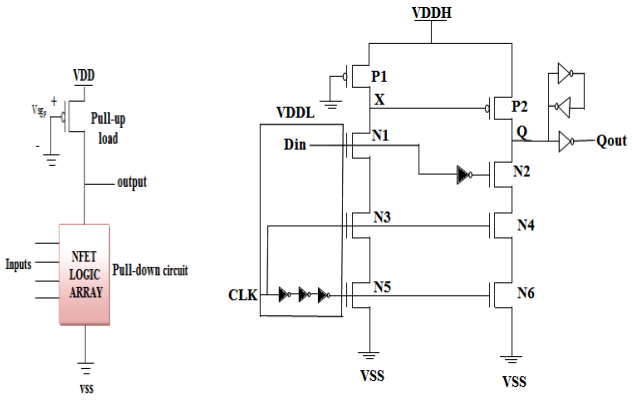
4 Operational Details and Implementation

The Differential level conversion scheme has large power consumption and delay overhead due to crossover contention ,pre-charging scheme reduces the delay but pre-charging node will consumes more power and NMOS pass transistor scheme normally has threshold voltage drop due that it will increases delay.

4.1 Conventional Clocked Pseudo n-MOS (CPN) LCFF

Fig 4.1.1(a) shows pseudo n-MOS scheme.CPN level shifting scheme use pseudo n-MOS technique to ensure the high speed operation with PMOS (P1) in the pull-up circuit is always it acts as a resistive load. Fig. 4.1.1(b) illustrates the clocked pseudo n-MOS Flip-Flop without using conditional discharging technique.

This level shifting scheme consumes power (18.191u) and delay (81.519p). When compare with above results power consumption is increases 18% and delay gets reduced 76%.Simulation results as shown below Fig. 4.1.2(a) and 4.1.2(b).



(a) (b)

Fig 4.1.1 (a) Pseudo n-MOS Logic, (b) Conventional Clocked Pseudo n-MOS Flip-Flop

4.1.2 Simulation Results of Conventional Clocked Pseudo n-MOS LCFF (CONV CPN-LCFF)

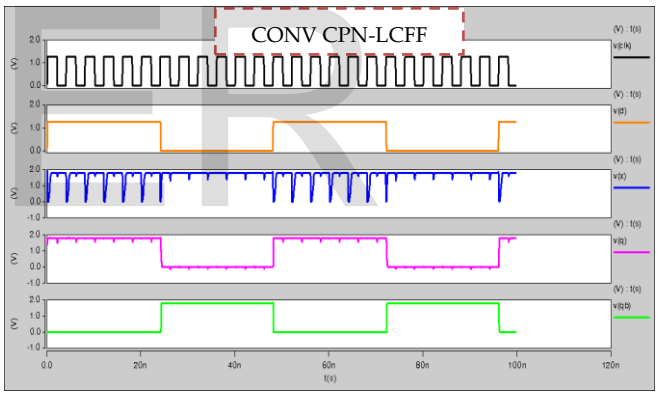


Fig 4.1.2 (a) Results of Data to Output (D-to-Q) for Conventional Clocked Pseudo n-MOS LCFF

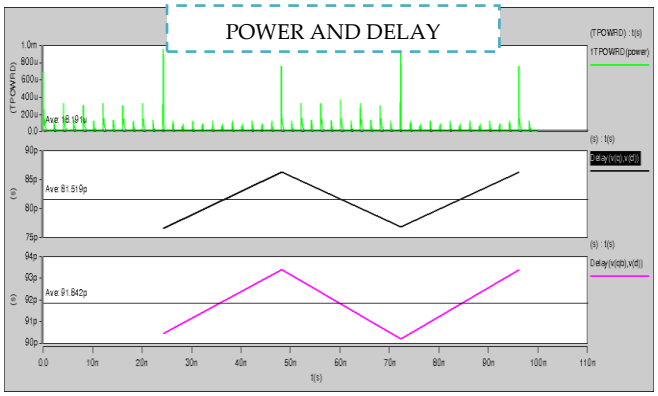


Fig 4.1.2 (b) Results of Power and Delay

However, drawback of this level-shifting scheme is that when input (Din) signal is remains high then the intermediate node X discharges at once and every clock cycle it makes unnecessary switching without generating useful activity at the output. This redundant switching

activity resulting in dynamic power dissipation it causes more power consumption.

- Techniques for reducing redundant switching activity
  - Conditional Capture Technique
  - Conditional pre-charge Technique
  - Conditional Discharge Technique

Conditional discharging technique as used to control the redundant switching activity in this pseudo n-MOS scheme [9, 10].

4.2 Clocked Pseudo n-MOS (CPN) LCFF

To further improvement on power, the clocked pseudo n-MOS level-shifting scheme has proposed in this scheme, which combines pseudo n-MOS technique to ensure high-speed operation with conditional discharge technique to reduce the redundant switching activity. Fig. 4.2.1 illustrates the Clocked pseudo n-MOS scheme.

When Din stays high a feedback signal (Q-fdb) MN7 transistor will be turn off to avoid unnecessary short–circuit power as well as the redundant switching activity at the intermediate node X. Although P1 always ON, short-circuit occurs during Din makes a transition of 0 -> 1 and discharge path is disconnected after two gates of delay.

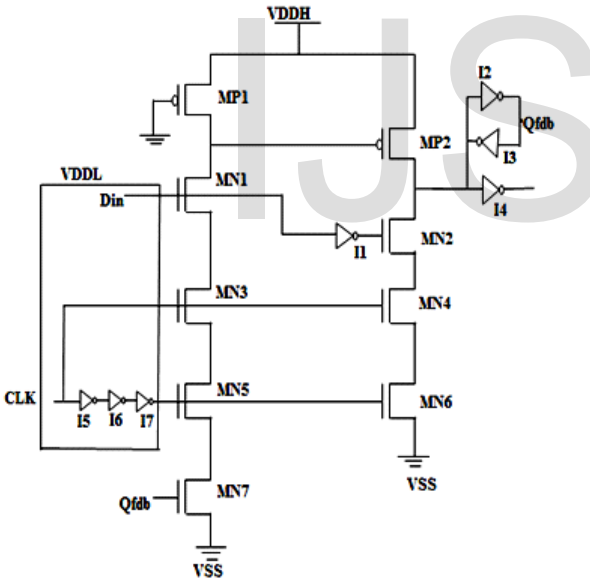


Fig 4.2.1 Clocked Pseudo n-MOS LCFF using Conditional Discharge scheme

This technique consumes power (13.179u) and delay (88.994p). When compare with above results power gets reduced 28% and Delay, 9.61% increased resulting in propagation delay. Simulation results as shown below Fig 4.2.2 (a) and Fig 4.2.2 (b).

Hence, due to this modification power consumption has significantly reduced. Since it resulting in complex clocking structure due to adding one more transistor Qfbd for reducing redundant switching activity and more number of transistors switches the clock, so it will results in increases the clock load, power consumption and parasitic capacitance.

4.2.2 Simulation Results of CPNMOS- LCFF

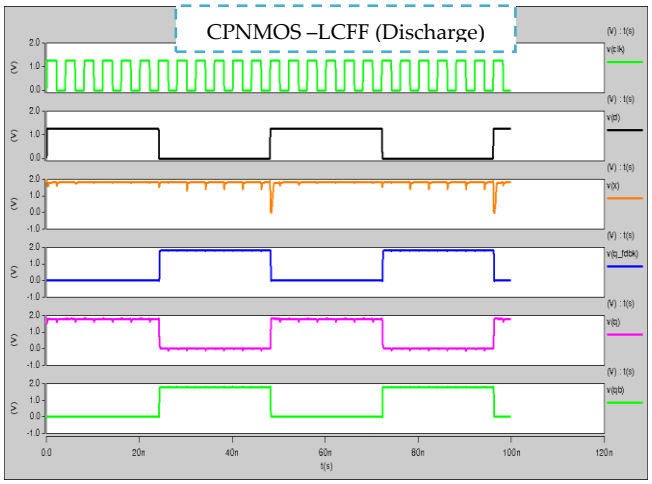


Fig 4.2.2 (a) Results of D-to-Q for CPNMOS-LCFF

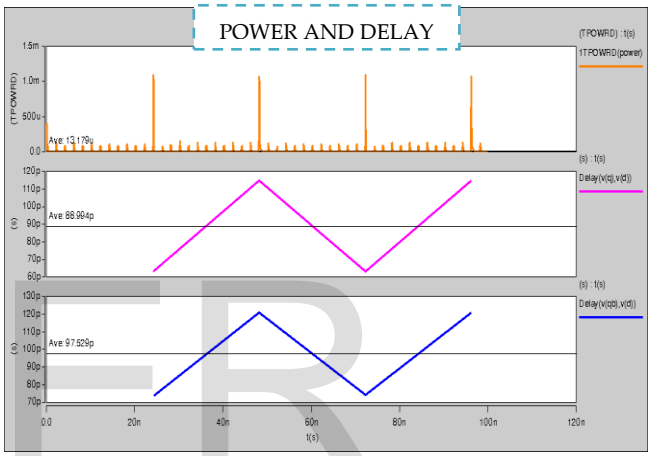


Fig 4.2.2(b) Results of Power and Delay for CPNMOS-LCFF

4.3 Proposed Clocked Sharing Pseudo n-MOS Level Conversion Flip-Flop (CSPN-LCFF)

To further attain high performance with reduced power consumption and delay overhead, the clocked sharing pseudo n-MOS (CS-PN) level shifting scheme is proposed. Fig 4.3.1 illustrates the sharing pseudo n-MOS technique as shown in below figure. This level shifting scheme, the p-MOS (MP1) is always ON which combines pseudo n-MOS logic for improve speed operation and conditional discharging scheme for reduced switching activity and sharing technique for reduced clocked distribution network.

To ensure the efficient implementation of the implicit –pulse triggered flip-flop and improve the problem associated with the previous designs, which is large propagation delay. In order to overcome this problem, the sharing technique as proposed in this circuit design. In which, the two clocked branches of (MN3, MN5) and (MN4, MN6) in the previous design (Fig 4.2.1) clocked transistors are merged to form single group of (MN3, MN4) and note that the split path (intermediate node X will not drive the transistor MN2 which is used as output discharging path in the second stage), so it will ensure correct functioning after merging the clocked transistors.

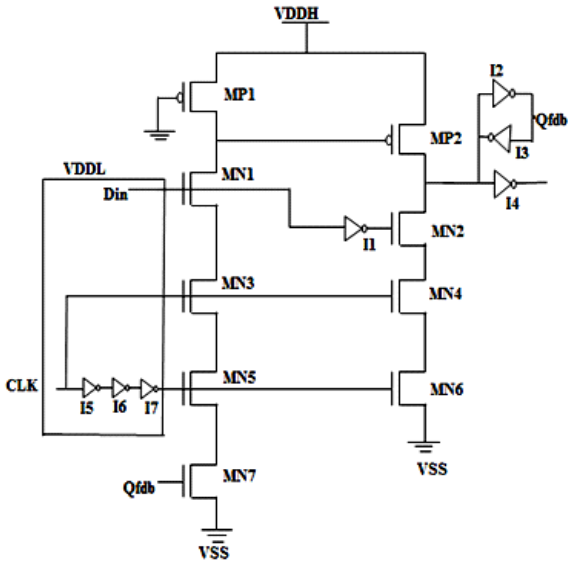


Fig. 4.3.1 Proposed Clocked Sharing Pseudo n-MOS LCFF

The importance of sharing concept in which it will reflect in reducing the number of clocked transistors required to implementing the clocking system because the clocked transistors consumes more power consumption due to 100% switching activity.

4.3.2 Simulation Results of CS-PN LCFF

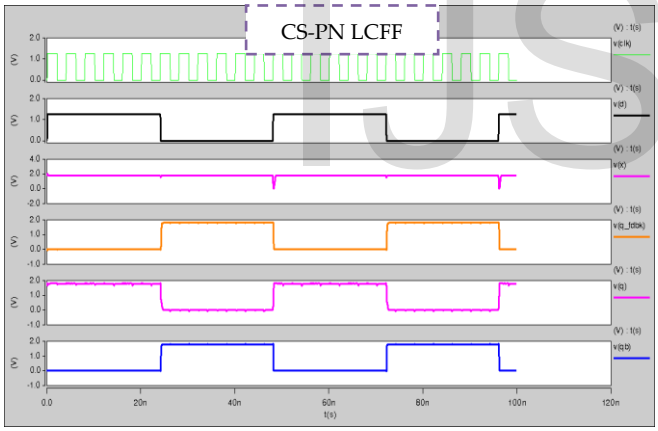


Fig 4.3.2 (a) Results of D-to-Q for CS-PN LCFF Scheme

Fig 4.7 (b) Results of Power and Delay for CS-PN LCFF

This scheme consumes power (11.555u) and delay (80.576p), when compare with above results sharing technique will gets reduce power 12.32% and delay 9.4%. Simulation results are shown in above Fig. 4.3.2(a) and Fig 4.3.2(b).

5 Experimental Results

All circuits are simulated using HSPICE simulation, in TSMC 0.18um and level 49-BSIM3 (version3) model and waveforms are viewed using Cosmos Scope for different nm technologies such as 180nm, 130nm, 90nm, and 65nm. A clock frequency 250MHz and lambda based design rule is used in thesis that the parameter of λ is half off the gate length.

Power consumed in the data and clock drivers are in our measurements. Circuits were optimized for Power Delay Product (PDP). Delay is data to output delay (D-to-Q) is the sum of the setup time and clock to the output Delay. The D-to-Q delay is obtained from sweeping the 0→1 and 1→0 data transition with respect to the clock edge.

5.1. Compare the Analysis of Pseudo n-MOS Logic

5.1.1 Switching Activity

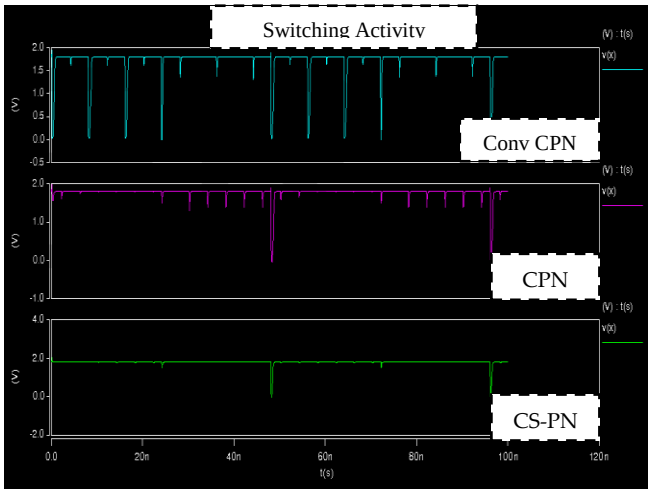


Fig 5.1.1.1 Switching Activities of Intermediate Node X

5.1.2 Delay

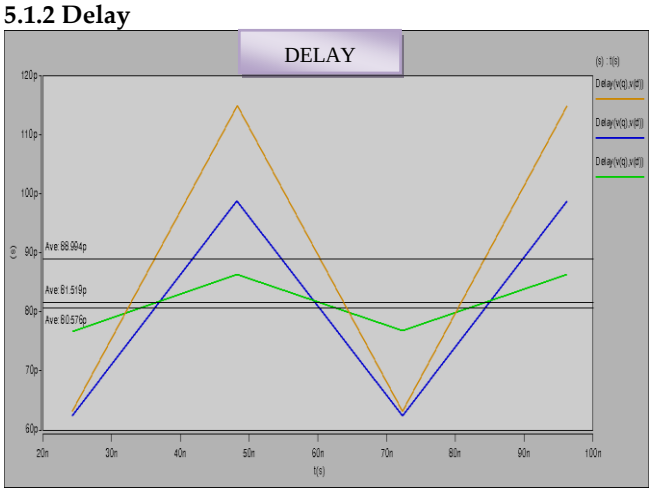


Fig 5.1.2.1 Delay Analysis of Pseudo n-MOS schemes

5.2 Simulation Results of Average Power in Different nm Technologies

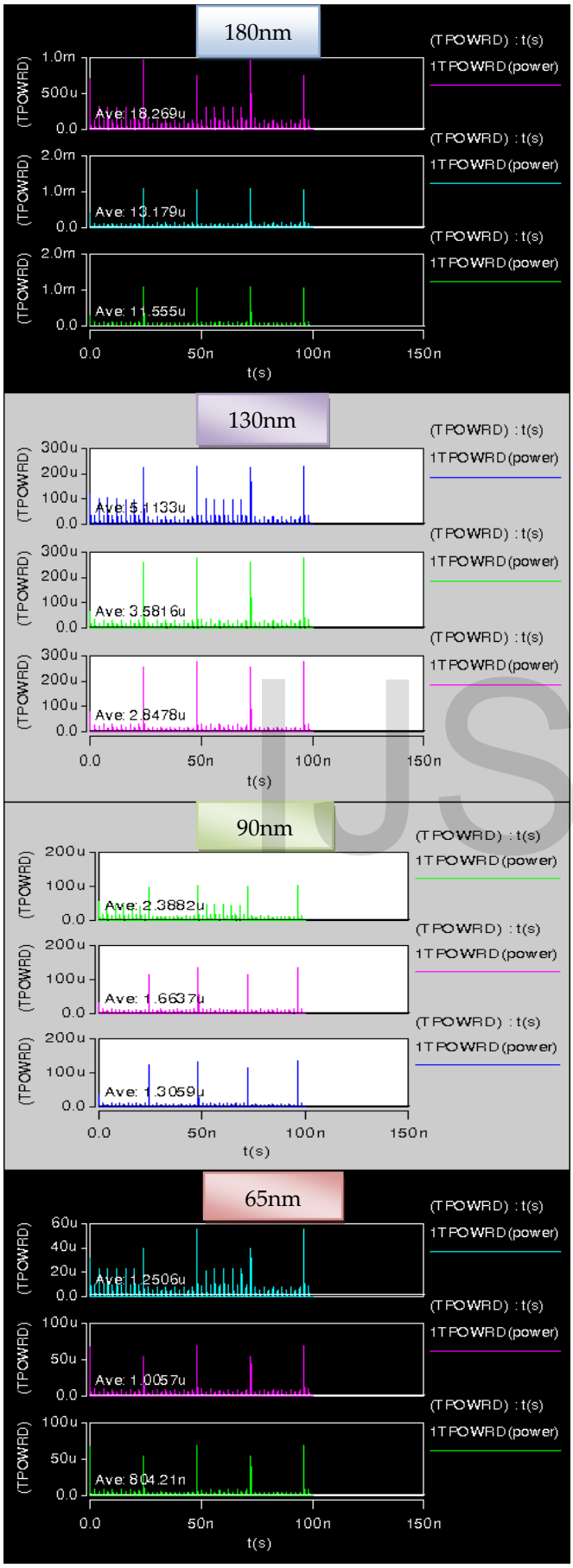
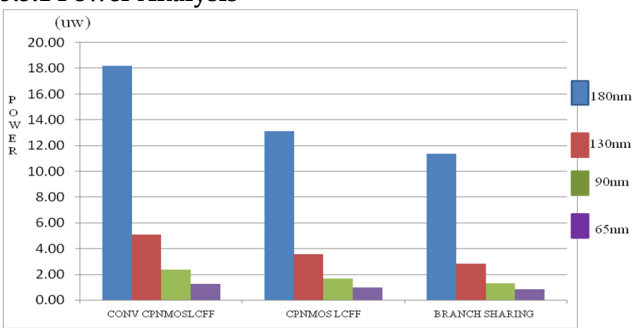


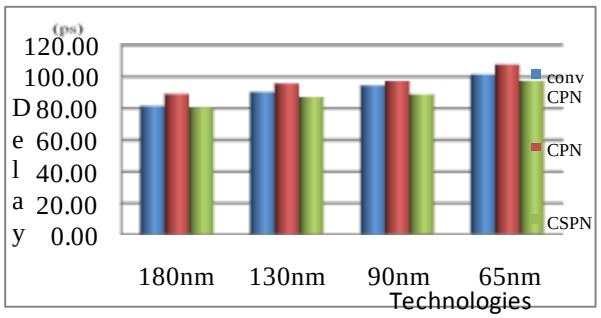
Fig 5.2.1 Compare Average Power in 180nm, 130nm, 90nm and 65nm Technologies

5.3 Graphical representation of Power delay product (PDP) analysis

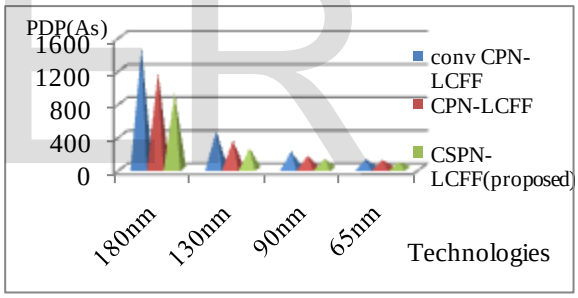
5.3.1 Power Analysis



5.3.2 Delay Analysis



5.3.3 Power Delay Product (PDP) Analysis



5.4 Flip-Flop Characteristics of Proposed CSPNMOS-LCFF for Different Deep submicron Technologies

	180nm	130nm	90nm	65nm
Power(μw)	11.375	2.847	1.3059	0.842
Delay(ps)	80.576	87.23	88.61	97.21
PDP(As)	918.64	248.34	123.36	85.33

6 Conclusion

The proposed clock sharing pseudo n-MOS (CS-PN) technique combines the pseudo n-MOS logic, conditional discharge and clock sharing technique. By this technique 10% of power and 9.5% of delay had been improved when compared with CPN LCFF, which is the main constraint of clustered voltage scaling (CVS) scheme.

By using 65nm submicron technology, PDP enhanced by approximately 50% as observed from simulation results.

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